

APPARATUS AND METHOD FOR STATE
SELECTABLE TRACE STREAM GENERATION

Abstract of the Invention

1 A trace test and debug system for a target processor
2 generates a program counter trace stream, a timing trace
3 stream and a data trace stream. The target processor has
4 three states, a program code execution state, an interrupt
5 service routine code execution state, and a state where
6 code execution is halted. The trace streams can be
7 controlled so that the timing trace stream can be generated
8 or excluded during the code execution halts. Similarly,
9 when the timing trace stream is enabled for the interrupt
10 service routine(s), the program counter and data trace
11 streams can be selectively generated or excluded. The
12 contents of the pipeline flattener can be held or flushed
13 code execution halt depending on whether the pipeline is
14 unprotected or protected. When the contents of the
15 pipeline flattener are held during a code halt, the program
16 counter trace stream and data trace stream is halted even
17 if the timing trace stream remains active. When the
18 contents of the pipeline flattener are flushed, the program
19 counter and data trace streams are continued into the
20 period of the code execution halt.